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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

NGUYEN, VINH P

ART UNIT PAPER NUMBER

2829

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/791,768

Applicant(s)

PROLL ET AL.

Examiner

VINH P. NGUYEN

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7,9-11-15 and 18 is/are rejected.
- 7) ☒ Claim(s) 8 and 17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 0304.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 4-7 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by El Ayat et al (Pat # 5,528,600) .

As to claims 4-5 and 13, El Ayat et al disclose an integrated circuit as shown in figure 1 having a plurality of modules (12a-12i) arranged in rows and columns, control buses (XSEL1-XSEL3) for operating and driving the modules (12a-12i) of a number of groups of connection locations (a particular row), operating the modules of the number of groups (each row) simultaneously and the groups being connected to an address and command bus (46,48,50) via a respective switch (34,36,38). It appears that all the modules of El Ayat et al are located on a substrate because El Ayat et al teach that the modules are part of an integrated circuit.

As to claim 6, the modules interchanges data via the assigned data bus (DTI) are operated and driven.

As to claim 7, it appears that the modules (12a-12i) are subjected to functional test.

As to claim 9, it appears that the modules of the groups (12a-12i) are connected to the address and command bus via the respective switch means (34,36,38).

3. Claims 1-2,10-11,13-16,18 are rejected under 35 U.S.C. 102(b) as being anticipated by El Ayat et al (Pat # 5,528,600) .

As to claims 1-2 ,10-11,13-14 and 18, El Ayat et al disclose an integrated circuit as shown in figure 1 having a plurality of modules (12a-12i) arranged in rows and columns, control buses (XSEL1-XSEL3) for operating and driving the modules (12a-12i) of a number of groups of connection locations (a particular row),operating the modules of the number of groups (each row) simultaneously and the groups being connected to an address and command bus (46,48,50) via a respective switch (34,36,38). It appears that all the modules of El Ayat et al are located on a substrate because El Ayat et al teach that the modules are part of an integrated circuit. Furthermore, each module has a data terminal (terminal receiving the Data test Bit “DTI” through data bus “line connected to DTI”), a control terminal (terminal receiving XSEL1-XSEL3) and an address and command terminal (terminal receiving YSEL1-YSEL3) connected to an address and command bus (line connected to terminal “42” and lines 22,24,26).

As to claim 15, it appears that the modules interchange data via the assigned data bus .

As to claim 16, it appears that the modules are subjected to a functional test on the same substrate.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 3,12,16 are rejected under 35 U.S.C. 103(a) as being unpatentable over El Ayat et al (Pat # 5,528,600) in view of Boardman et al (Pat # 5,682,472).

El Ayat et al disclose an integrated circuit as shown in figure 1 as mentioned in paragraph # 3 above. El Ayat et al do not mention about the substrate in the form of a burn in board. As to claims 3,12 and 16, Boardman teach that functional test and the burn-in test are performed on the same device under test (see column 4, lines 54-57). It would have been obvious for one of ordinary skill in the art to recognize that the device under test on the carrier of El Ayat et al would be used in burn-in test as taught by Boardman et al, therefore, the carrier substrate of El Ayat et al would be qualified as "a burn-in test board" as taught by Boardman et al.

6. Claims 8 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art does not teach that the modules are operated at a first operating frequency in the burn-in test and at a second operating frequency in the functional test, the first operating frequency being smaller than the second operating frequency.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Baeg et al (pat # 5,519,713) disclose integrated circuit having clock line control and method for testing same.

El Ayat et al (pat # 4,857,774) disclose testing apparatus and diagnostic method for use with programmable interconnect architecture.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VINH P. NGUYEN whose telephone number is 571-272-1964.

The examiner can normally be reached on 6:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

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system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



VINH P NGUYEN

Primary Examiner

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04/01/05